

P-Channel Enhancement Mode Power MOSFET

<p>Description</p> <p>The GT2K0P20KA uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.</p> <p>AEC-Q101 Qualified</p> <p>General Features</p> <ul style="list-style-type: none"> ● V_{DS} -200V ● I_D (at $V_{GS} = -10V$) -18A ● $R_{DS(ON)}$ (at $V_{GS} = -10V$) < 220mΩ ● $R_{DS(ON)}$ (at $V_{GS} = -4.5V$) < 230mΩ ● 100% Avalanche Tested ● RoHS Compliant <p>Application</p> <ul style="list-style-type: none"> ● Power switch ● DC/DC converters 	<p>Schematic diagram</p> <p>TO-252</p>
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Ordering Information			
Device	Package	Marking	Packaging
GT2K0P20KA	TO-252	GT2K0P20	2500pcs/Reel

Absolute Maximum Ratings $T_C = 25^\circ C$, unless otherwise noted			
Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-200	V
Continuous Drain Current	I_D	-18	A
Pulsed Drain Current (note1)	I_{DM}	-72	A
Gate-Source Voltage	V_{GS}	± 20	V
Power Dissipation	P_D	138	W
Single pulse avalanche energy (note2)	E_{AS}	144	mJ
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 To 150	°C

Thermal Resistance			
Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient	R_{thJA}	50	°C/W
Maximum Junction-to-Case	R_{thJC}	0.9	°C/W

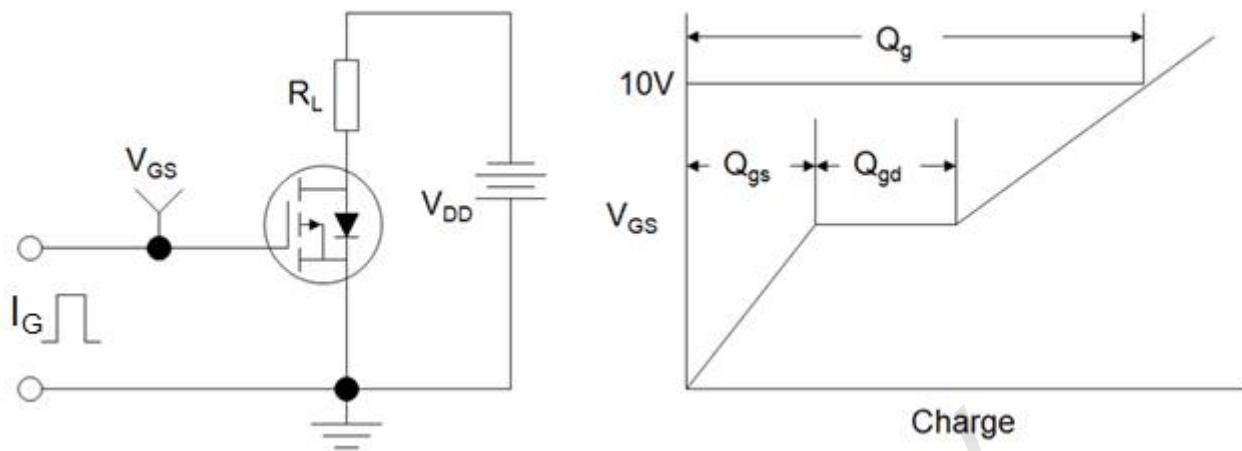
Specifications $T_J = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = -250\mu\text{A}$	-200	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}} = -200\text{V}, V_{\text{GS}} = 0\text{V}$	--	--	-1	μA
Gate-Source Leakage	I_{GSS}	$V_{\text{GS}} = \pm 20\text{V}$	--	--	± 100	nA
Gate-Source Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}} = V_{\text{GS}}, I_D = -250\mu\text{A}$	-1.0	-2.0	-3.0	V
Drain-Source On-Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = -10\text{V}, I_D = -15\text{A}$	--	180	220	$\text{m}\Omega$
		$V_{\text{GS}} = -4.5\text{V}, I_D = -15\text{A}$	--	190	230	
Forward Transconductance	g_{FS}	$V_{\text{DS}} = -5\text{V}, I_D = -15\text{A}$	--	20	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = -100\text{V}, f = 1.0\text{MHz}$	--	3400	--	pF
Output Capacitance	C_{oss}		--	100	--	
Reverse Transfer Capacitance	C_{rss}		--	10	--	
Total Gate Charge	Q_g	$V_{\text{DD}} = -100\text{V}, I_D = -15\text{A}, V_{\text{GS}} = -10\text{V}$	--	70	--	nC
Gate-Source Charge	Q_{gs}		--	12	--	
Gate-Drain Charge	Q_{gd}		--	19	--	
Turn-on Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}} = -100\text{V}, I_D = -15\text{A}, R_G = 1.6\Omega$	--	16	--	ns
Turn-on Rise Time	t_r		--	10	--	
Turn-off Delay Time	$t_{\text{d}(\text{off})}$		--	45	--	
Turn-off Fall Time	t_f		--	9	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	$T_C = 25^\circ\text{C}$	--	--	-18	A
Body Diode Voltage	V_{SD}	$T_J = 25^\circ\text{C}, I_{\text{SD}} = -15\text{A}, V_{\text{GS}} = 0\text{V}$	--	--	-1.2	V
Reverse Recovery Charge	Q_{rr}	$I_F = -15\text{A}, V_{\text{GS}} = 0\text{V}$ $dI/dt = -100\text{A/us}$	--	350	--	nC
Reverse Recovery Time	T_{rr}		--	80	--	ns

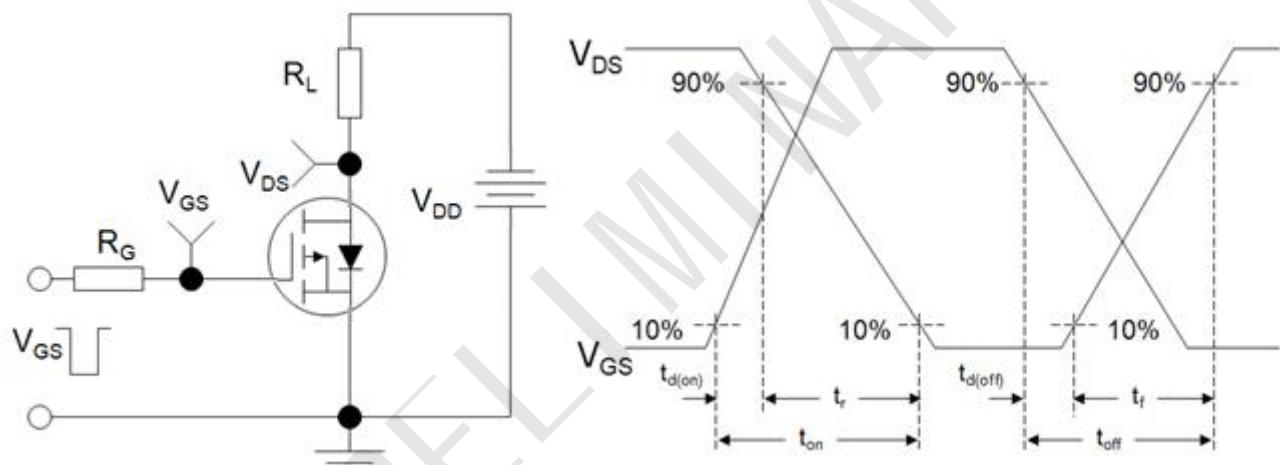
Notes

- Repetitive Rating: Pulse width limited by maximum junction temperature
- EAS condition : $T_J=25^\circ\text{C}$, $V_{\text{DD}}=-50\text{V}$, $V_{\text{GS}}=-10\text{V}$, $L=0.5\text{mH}$, $R_g=25\Omega$
The table shows the minimum avalanche energy, which is 400mJ when the device is tested until failure
- Identical low side and high side switch with identical R_g

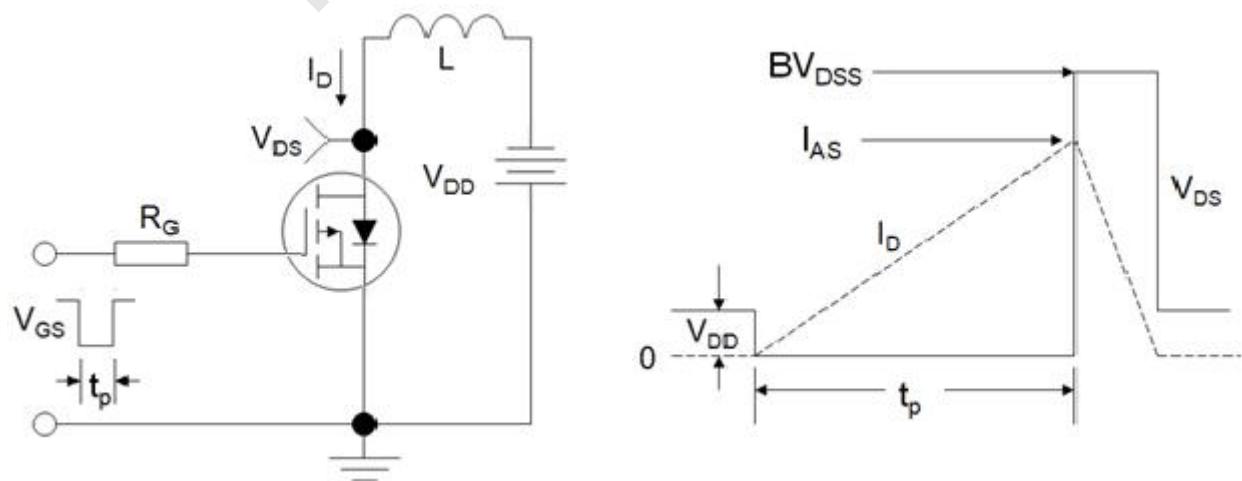
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 1. Output Characteristics

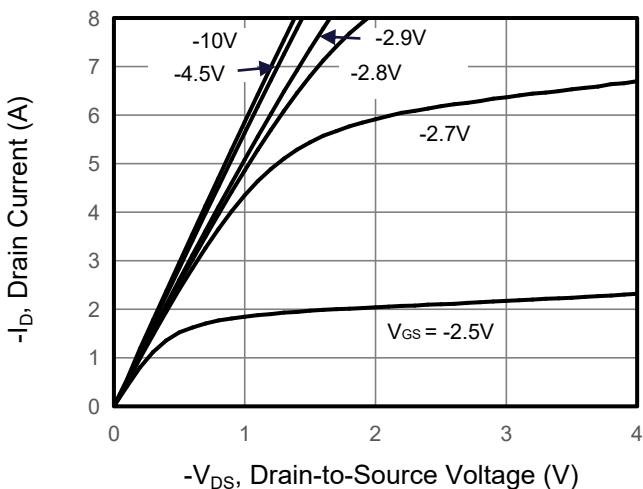


Figure 2. Transfer Characteristics

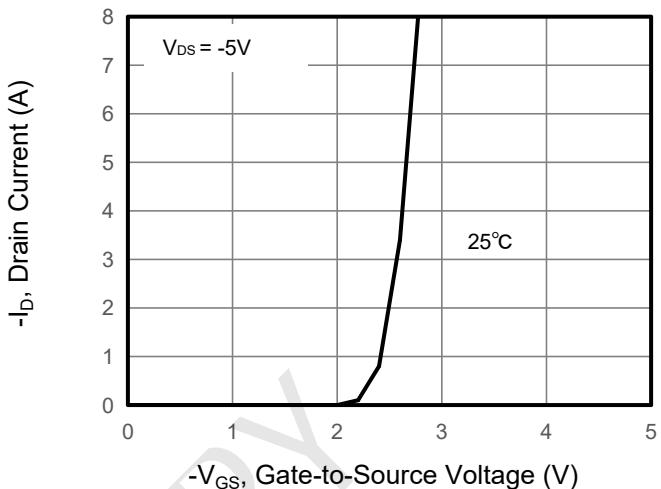


Figure 3. Drain Source On Resistance

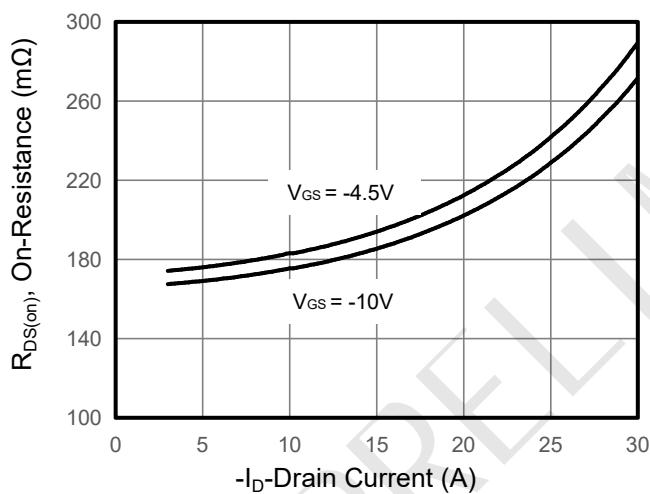


Figure 4. Gate Charge

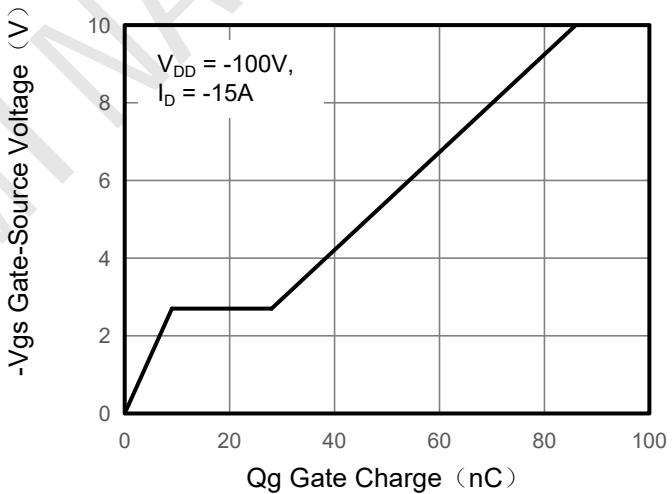


Figure 5. Capacitance

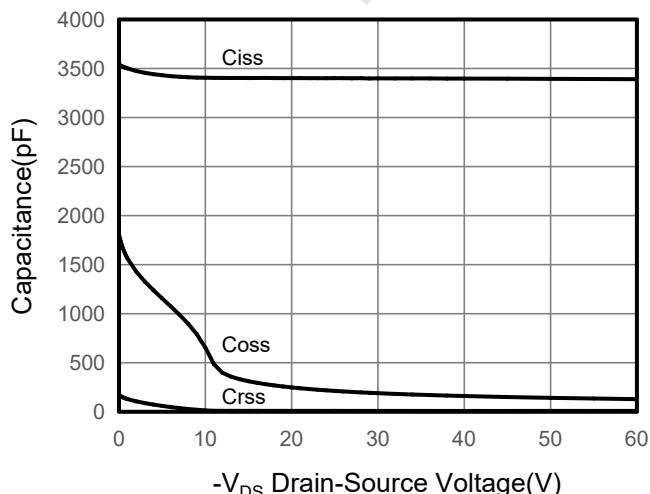
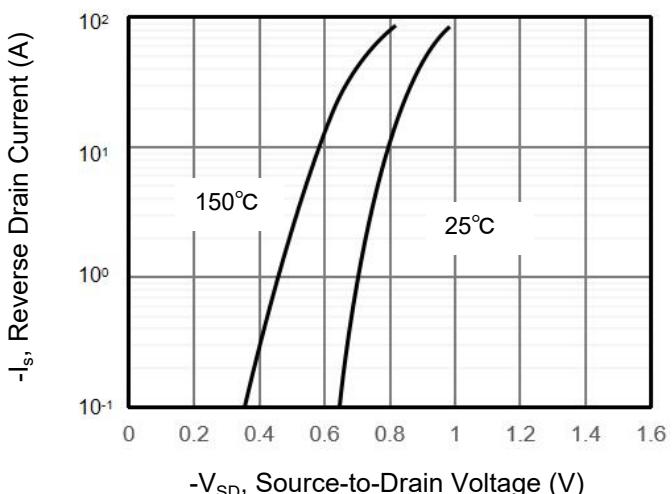


Figure 6. Source-Drain Diode Forward



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 7. Drain-Source On-Resistance

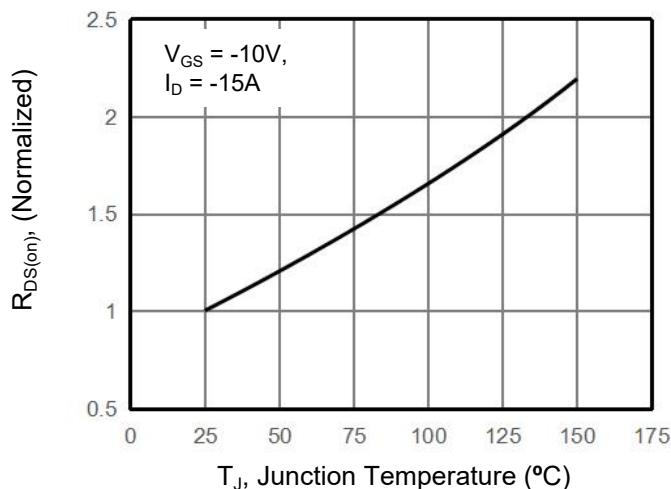


Figure 10. Safe Operation Area

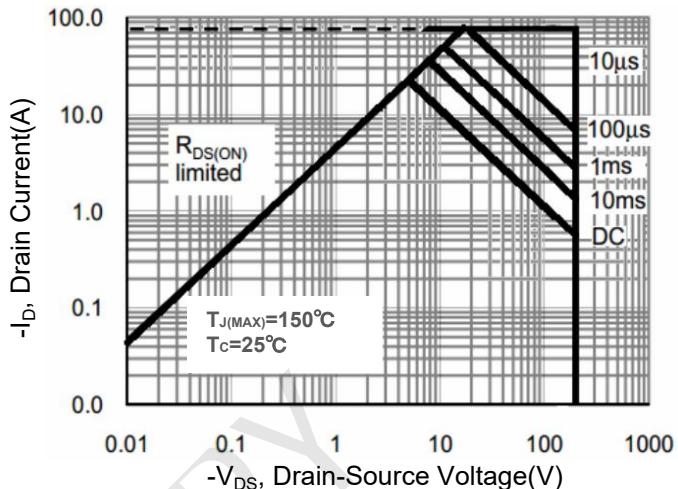
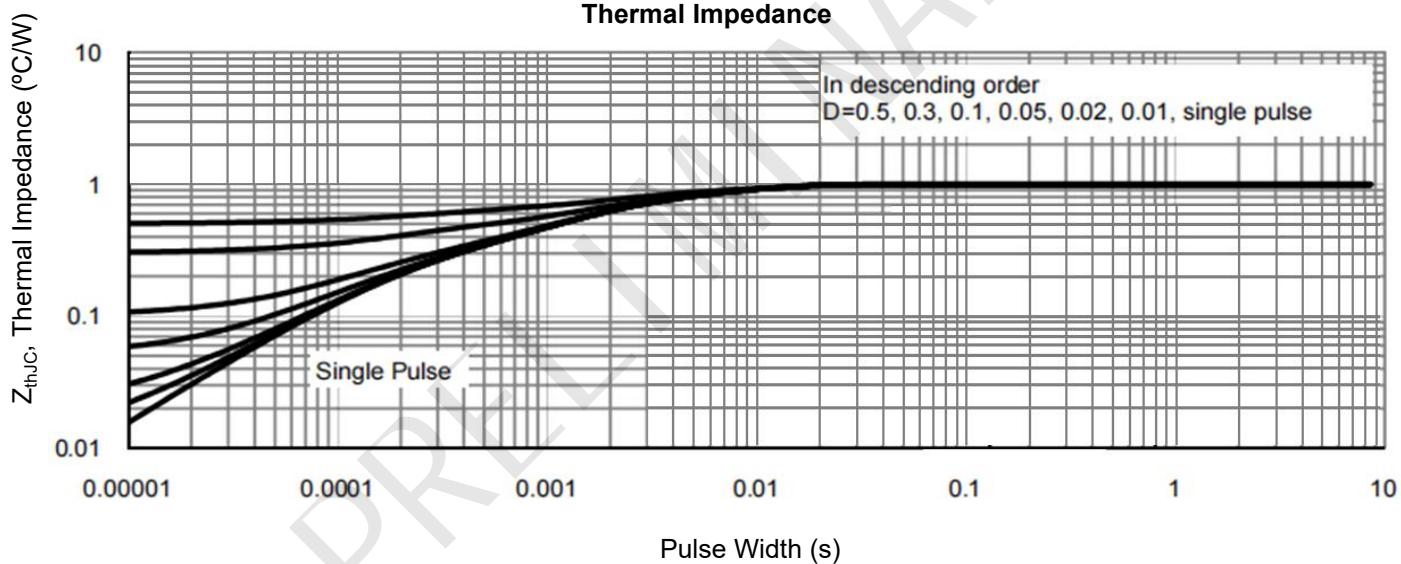
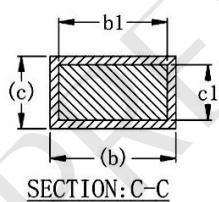
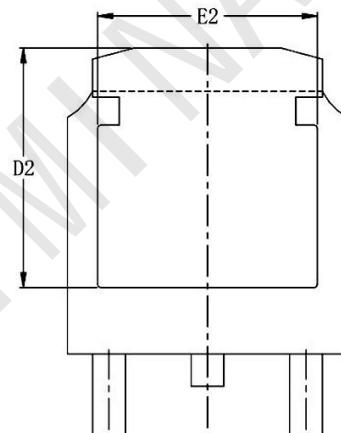
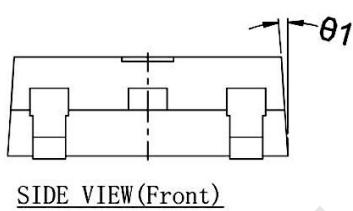
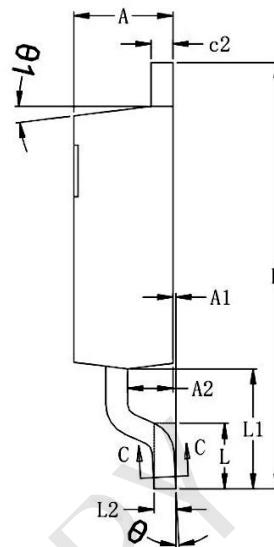
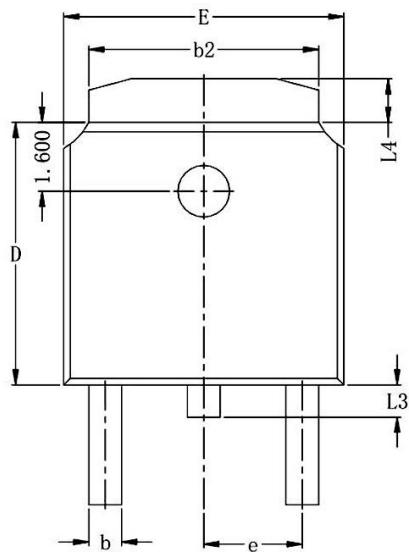


Figure 9. Normalized Maximum Transient Thermal Impedance



TO-252 Package Information



DIM SYMBOL	MIN.	NOM.	MAX.	DIM SYMBOL	MIN.	NOM.	MAX.
A	2.200	2.300	2.400	E	6.400	6.500	6.600
A1	0.000	0.070	0.130	E2	4.900	5.100	5.300
A2	0.950	1.050	1.150	e	2.286 BSC.		
b	0.700	0.800	0.900	H	9.700	9.900	10.100
b1	0.660	0.760	0.860	L	1.380	1.525	1.725
b2	5.134	5.334	5.534	L1	2.588	2.788	2.988
c	0.448	0.548	0.648	L2	0.508 BSC.		
c1	0.458	0.508	0.558	L3	0.600	0.750	0.950
c2	0.448	0.548	0.648	L4	0.812	1.012	1.212
D	6.000	6.100	6.200	theta	1°	3°	5°
D2	5.372	5.572	5.772	theta1	6°	7°	8°