

N-Channel Enhancement Mode Power MOSFET

Description

The GT048N10TA uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.

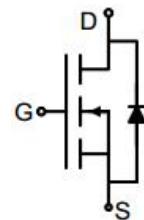
AEC-Q101 Qualified

General Features

- V_{DS} 100V
- I_D (at $V_{GS} = 10V$) 110A
- $R_{DS(ON)}$ (at $V_{GS} = 10V$) < 4.8mΩ
- $R_{DS(ON)}$ (at $V_{GS} = 4.5V$) < 6.5mΩ
- 100% Avalanche Tested
- RoHS Compliant

Application

- Power switch
- DC/DC converters



Schematic diagram



TO-220

Ordering Information

Device	Package	Marking	Packaging
GT048N10TA	TO-220	GT048N10	50pcs/Tube

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	100	V
Continuous Drain Current $T_C = 25^\circ\text{C}$	I_D	110	A
$T_C = 100^\circ\text{C}$		70	
Pulsed Drain Current (note1)	I_{DM}	440	A
Gate-Source Voltage	V_{GS}	± 20	V
Power Dissipation	P_D	150	W
Single pulse avalanche energy (note2)	E_{AS}	210	mJ
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 To 150	°C

Thermal Resistance

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient	R_{thJA}	50	°C/W
Thermal Resistance, Junction-to-Case	R_{thJC}	0.83	°C/W

Specifications $T_J = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$	100	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}} = 100\text{V}, V_{\text{GS}} = 0\text{V}$	--	--	1	μA
Gate-Source Leakage	I_{GSS}	$V_{\text{GS}} = \pm 20\text{V}$	--	--	± 100	nA
Gate-Source Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}} = V_{\text{GS}}, I_D = 250\mu\text{A}$	1.0	1.7	2.5	V
Drain-Source On-Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 10\text{V}, I_D = 20\text{A}$	--	4.4	4.8	$\text{m}\Omega$
		$V_{\text{GS}} = 4.5\text{V}, I_D = 20\text{A}$	--	5.2	6.5	
Forward Transconductance	g_{FS}	$V_{\text{GS}} = 5\text{V}, I_D = 20\text{A}$	--	49	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 50\text{V}, f = 0.8\text{MHz}$	--	3220	--	pF
Output Capacitance	C_{oss}		--	1225	--	
Reverse Transfer Capacitance	C_{rss}		--	9	--	
Total Gate Charge	Q_g	$V_{\text{DD}} = 50\text{V}, I_D = 20\text{A}, V_{\text{GS}} = 10\text{V}$	--	68	--	nC
Gate-Source Charge	Q_{gs}		--	8	--	
Gate-Drain Charge	Q_{gd}		--	16	--	
Turn-on Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}} = 50\text{V}, I_D = 20\text{A}, R_G = 2.2\Omega$	--	13	--	ns
Turn-on Rise Time	t_r		--	27	--	
Turn-off Delay Time	$t_{\text{d}(\text{off})}$		--	24	--	
Turn-off Fall Time	t_f		--	5	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	$T_C = 25^\circ\text{C}$	--	--	110	A
Body Diode Voltage	V_{SD}	$T_J = 25^\circ\text{C}, I_{\text{SD}} = 20\text{A}, V_{\text{GS}} = 0\text{V}$	--	--	1.2	V
Reverse Recovery Charge	Q_{rr}	$I_F = 20\text{A}, V_{\text{GS}} = 0\text{V}$ $dI/dt = 600\text{A/us}$	--	116	--	nC
Reverse Recovery Time	T_{rr}		--	25	--	ns

Notes

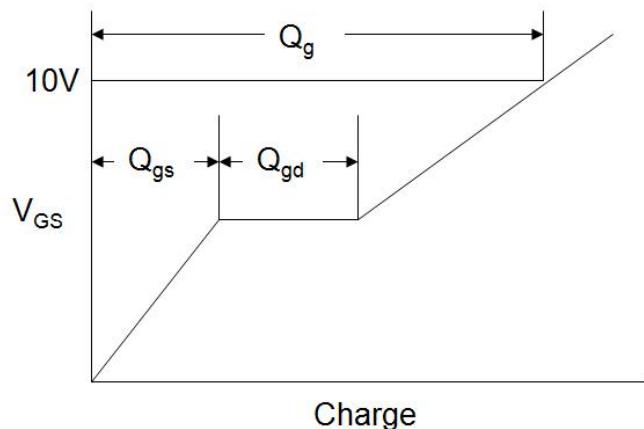
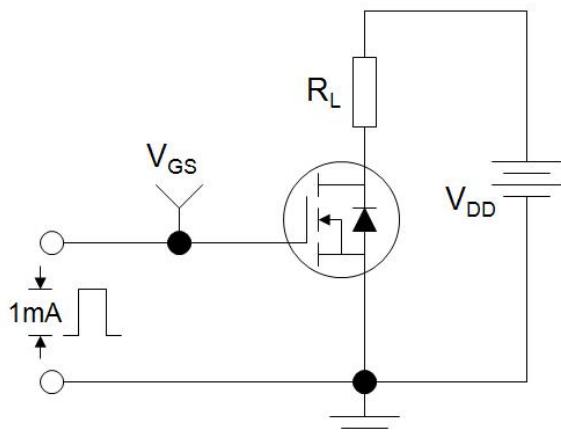
1. Repetitive Rating: Pulse width limited by maximum junction temperature

2. EAS condition : $T_J=25^\circ\text{C}$, $V_{\text{DD}}=50\text{V}$, $V_{\text{GS}}=10\text{V}$, $L=0.5\text{mH}$, $R_G=25\Omega$

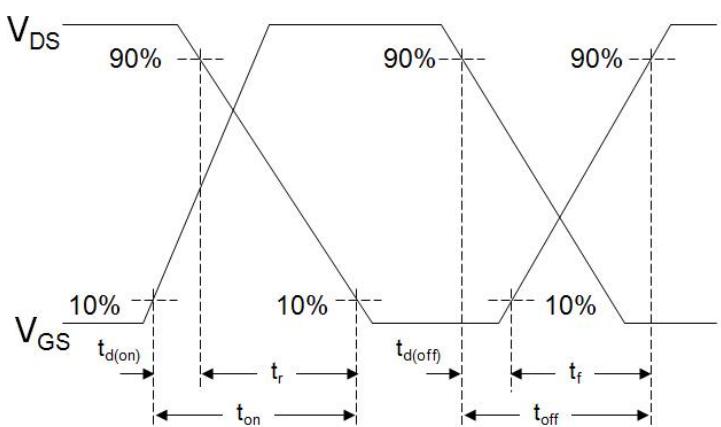
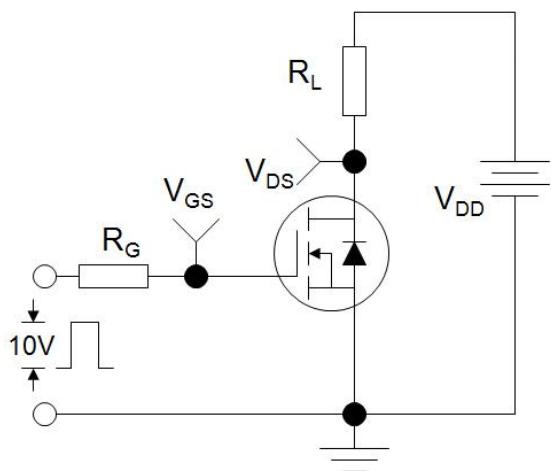
The table shows the minimum avalanche energy, which is 570mJ when the device is tested until failure

3. Identical low side and high side switch with identical R_G

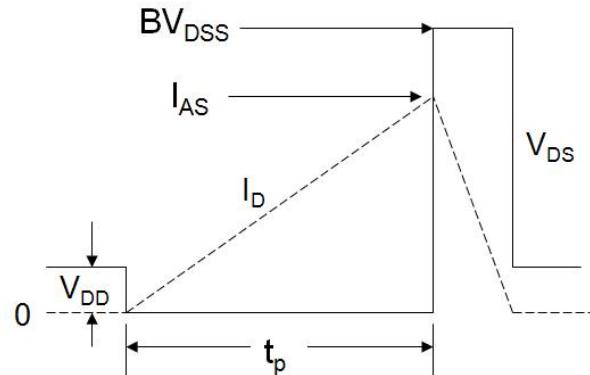
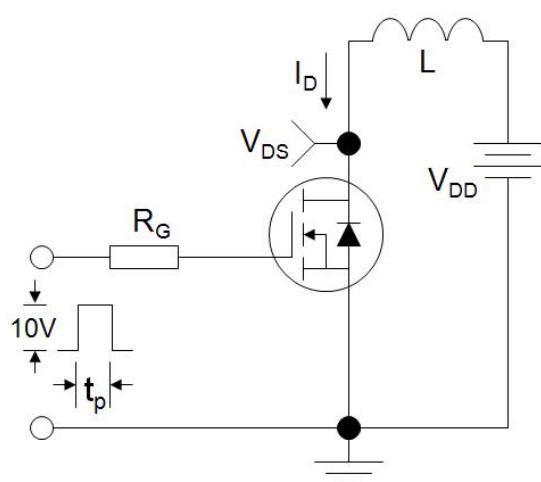
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 1. Output Characteristics

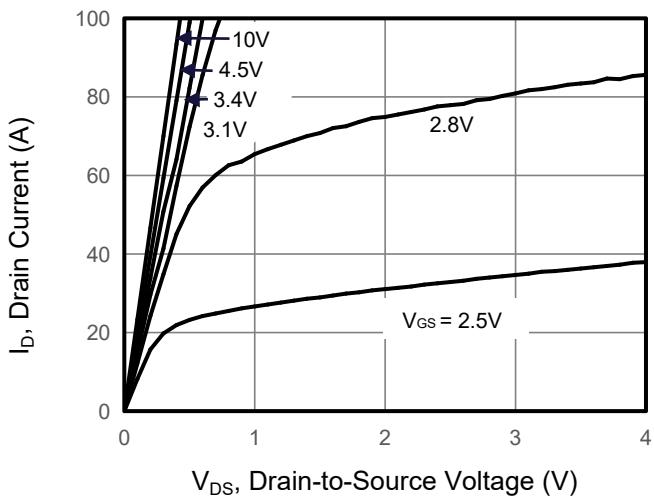


Figure 2. Transfer Characteristics

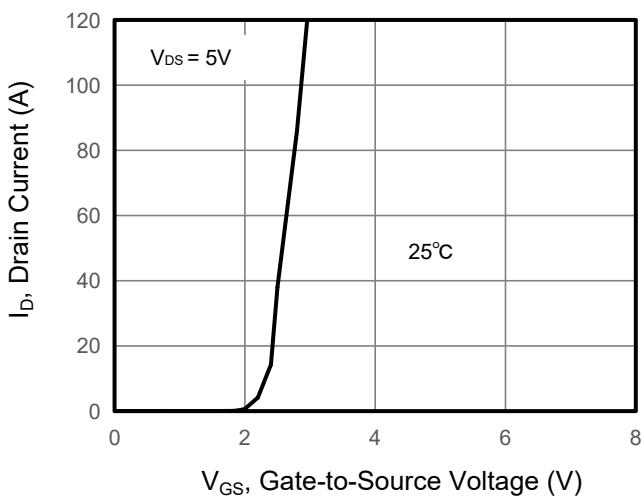


Figure 3. Drain Source On Resistance

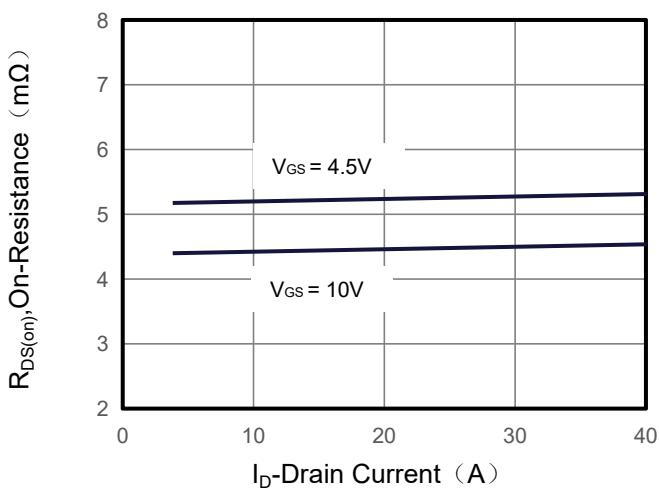


Figure 4. Gate Charge

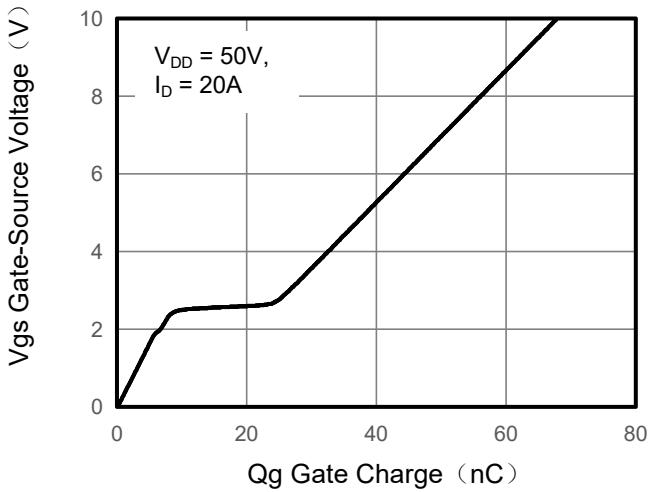


Figure 5. Capacitance

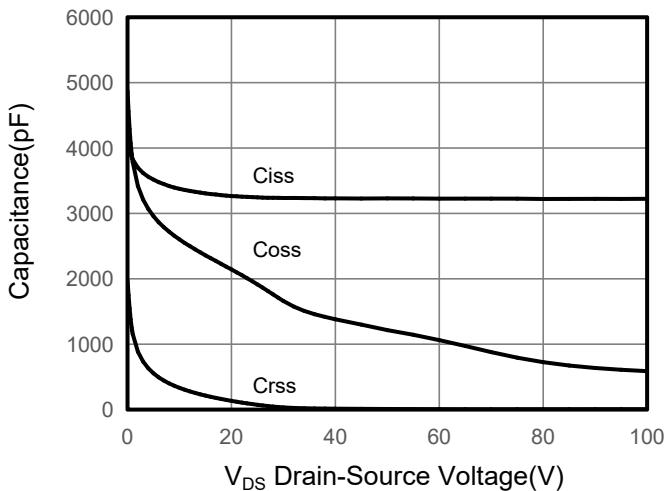
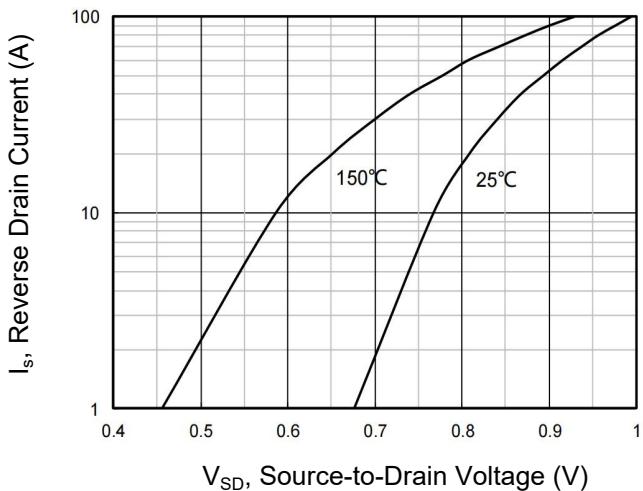


Figure 6. Source-Drain Diode Forward



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 7. Drain-Source On-Resistance

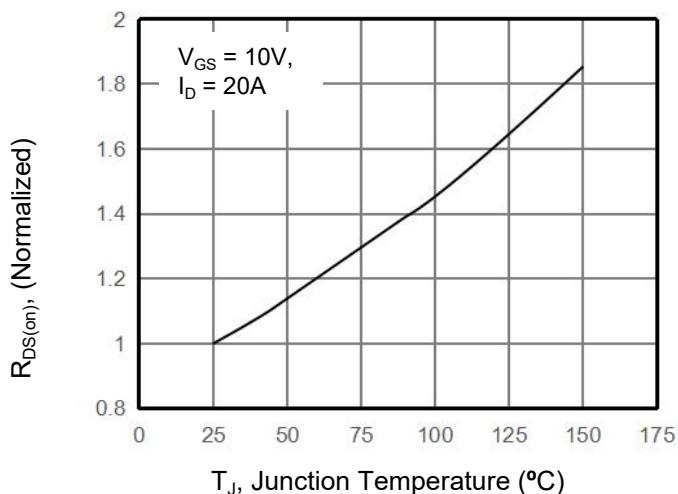


Figure 8. Safe Operation Area

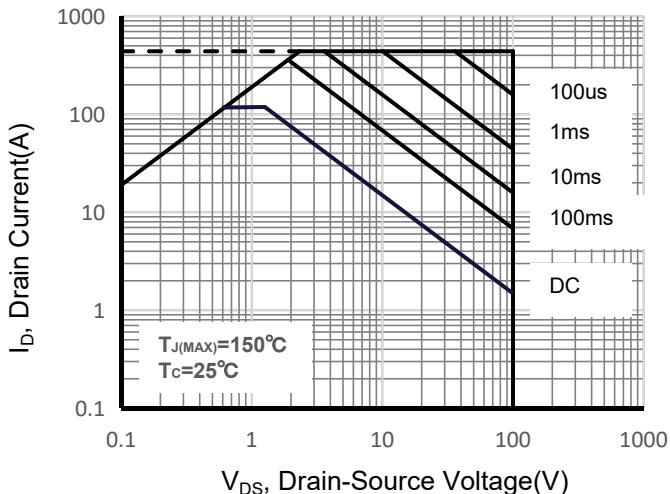


Figure 9. Maximum Continuous Drain Current vs Case Temperature

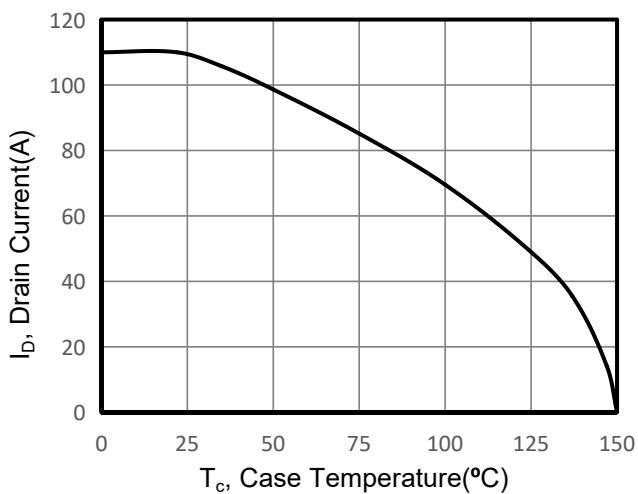
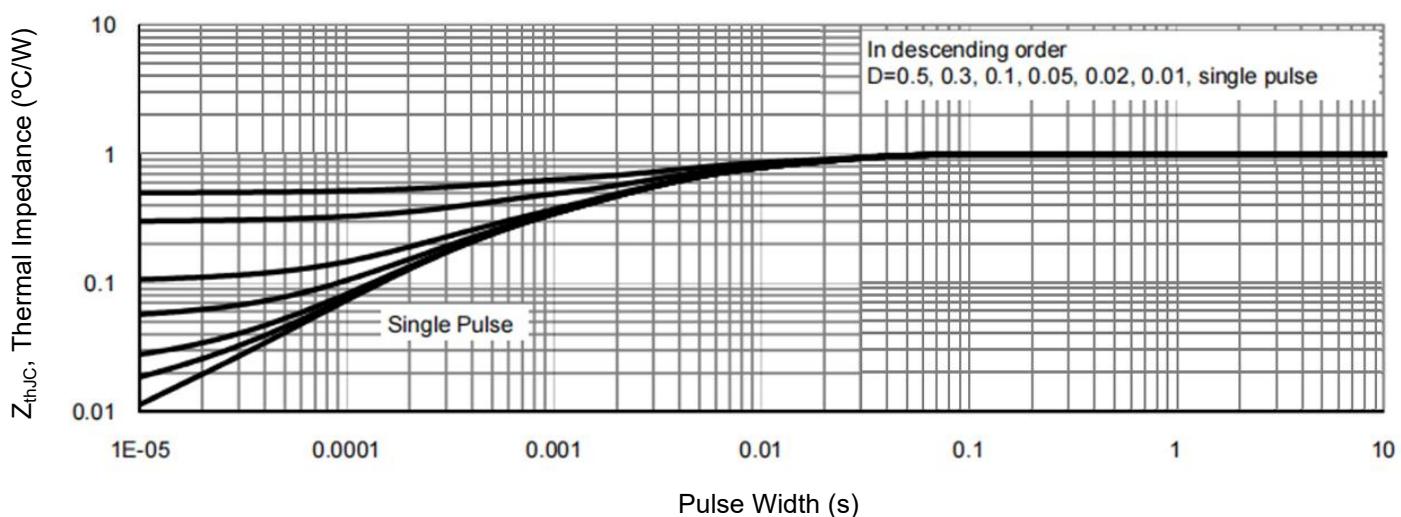
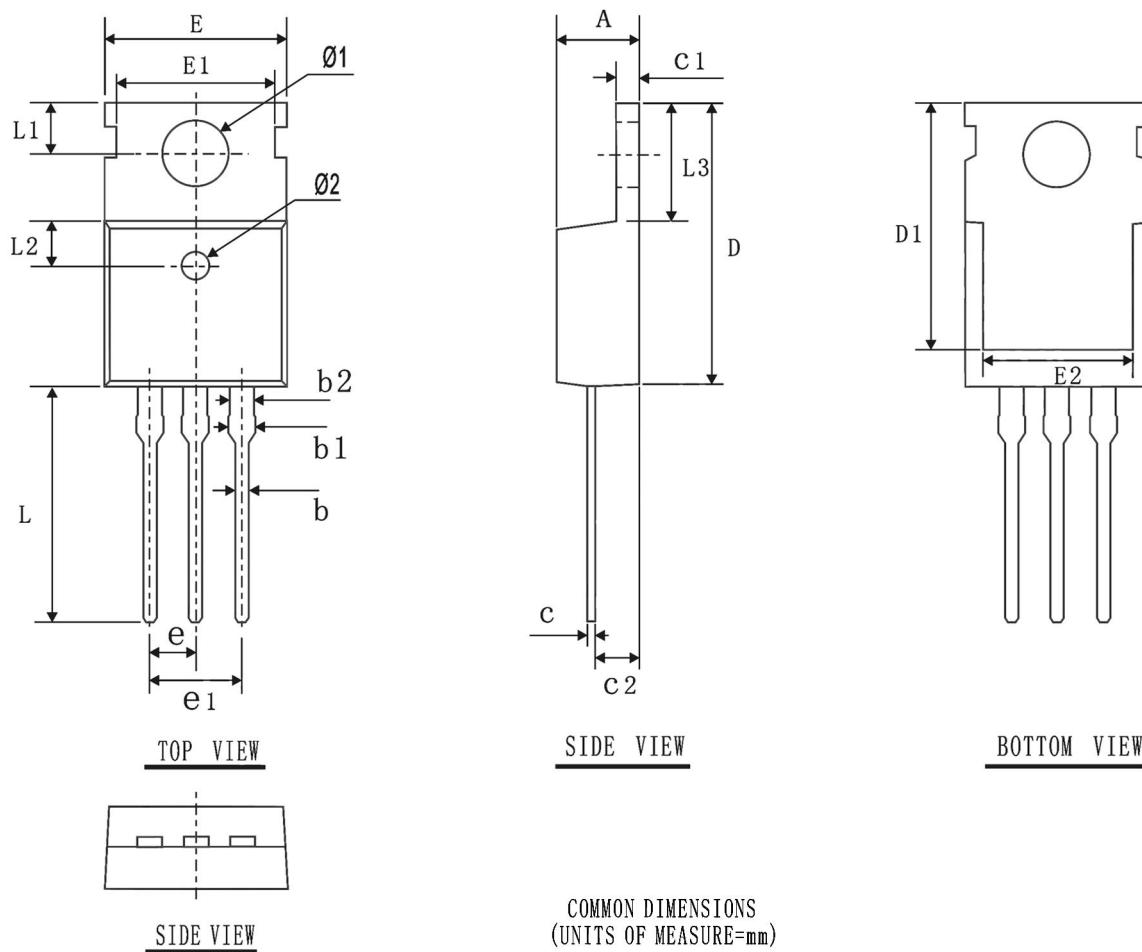


Figure 10. Normalized Maximum Transient Thermal Impedance



TO-220 Package Information



SYMBOL	MIN	NOM	MAX
A	4.30	4.50	4.70
b	0.70	0.80	0.90
b1	---	---	1.42
b2	1.17	1.27	1.37
c	0.40	0.50	0.60
C1	1.25	1.30	1.35
C2	2.20	2.40	2.60
D	15.45	15.65	15.85
D1	13.20	13.40	13.60
E	9.80	10.0	10.2
E1	8.60	8.70	8.80
E2	7.80	8.00	8.20
e1	4.88	5.08	5.28
L	12.95	13.15	13.35
L1	2.70	2.80	2.90
L2	2.40	2.50	2.60
L3	6.30	6.50	6.70
Ø1	3.50	3.60	3.70
Ø2	1.35	1.50	1.65
e	2.54BSC		