

P-Channel Enhancement Mode Power MOSFET

Description

The G12P10KEA uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.

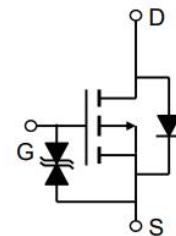
AEC-Q101 Qualified

General Features

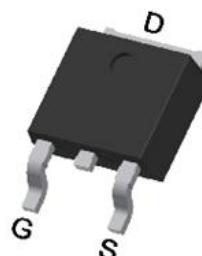
- V_{DS} -100V
- I_D (at $V_{GS} = -10V$) -12A
- $R_{DS(ON)}$ (at $V_{GS} = -10V$) < 200mΩ
- $R_{DS(ON)}$ (at $V_{GS} = -4.5V$) < 250mΩ
- 100% Avalanche Tested
- RoHS Compliant
- ESD (HBM) : 7.0KV

Application

- Power switch
- DC/DC converters



Schematic diagram



TO-252

Ordering Information

Device	Package	Marking	Packaging
G12P10KEA	TO-252	G12P10	2500pcs/Reel

Absolute Maximum Ratings $T_C = 25^\circ C$, unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-100	V
Continuous Drain Current $T_C = 25^\circ C$	I_D	-12	A
$T_C = 100^\circ C$		-7.5	
Pulsed Drain Current (note1)	I_{DM}	-48	A
Gate-Source Voltage	V_{GS}	± 20	V
Power Dissipation	P_D	45	W
Single pulse avalanche energy (note2)	E_{AS}	25	mJ
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 To 150	°C

Thermal Resistance

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient	R_{thJA}	55	°C/W
Thermal Resistance, Junction-to-Case	R_{thJC}	2.8	°C/W

Specifications $T_J = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = -250\mu\text{A}$	-100	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}} = -100\text{V}, V_{\text{GS}} = 0\text{V}$	--	--	-1	μA
Gate-Source Leakage	I_{GSS}	$V_{\text{GS}} = \pm 20\text{V}$	--	--	± 10	μA
Gate-Source Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}} = V_{\text{GS}}, I_D = -250\mu\text{A}$	-1.0	-1.7	-3.0	V
Drain-Source On-Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = -10\text{V}, I_D = -6\text{A}$	--	178	200	$\text{m}\Omega$
		$V_{\text{GS}} = -4.5\text{V}, I_D = -6\text{A}$	--	192	250	
Forward Transconductance	g_{FS}	$V_{\text{DS}} = -15\text{V}, I_D = -6\text{A}$	--	12	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = -50\text{V}, f = 1.0\text{MHz}$	--	1700	--	pF
Output Capacitance	C_{oss}		--	50	--	
Reverse Transfer Capacitance	C_{rss}		--	45	--	
Total Gate Charge	Q_g	$V_{\text{DD}} = -50\text{V}, I_D = -6\text{A}, V_{\text{GS}} = -10\text{V}$	--	32	--	nC
Gate-Source Charge	Q_{gs}		--	5	--	
Gate-Drain Charge	Q_{gd}		--	7	--	
Turn-on Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}} = -50\text{V}, I_D = -6\text{A}, R_G = 9\Omega$	--	52	--	ns
Turn-on Rise Time	t_r		--	12	--	
Turn-off Delay Time	$t_{\text{d}(\text{off})}$		--	38	--	
Turn-off Fall Time	t_f		--	28	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	$T_C = 25^\circ\text{C}$	--	--	-12	A
Body Diode Voltage	V_{SD}	$T_J = 25^\circ\text{C}, I_{\text{SD}} = -6\text{A}, V_{\text{GS}} = 0\text{V}$	--	--	-1.2	V
Reverse Recovery Charge	Q_{rr}	$I_F = -6\text{A}, V_{\text{GS}} = 0\text{V}$ $dI/dt = -500\text{A/us}$	--	35	--	nC
Reverse Recovery Time	T_{rr}		--	46	--	ns

Notes

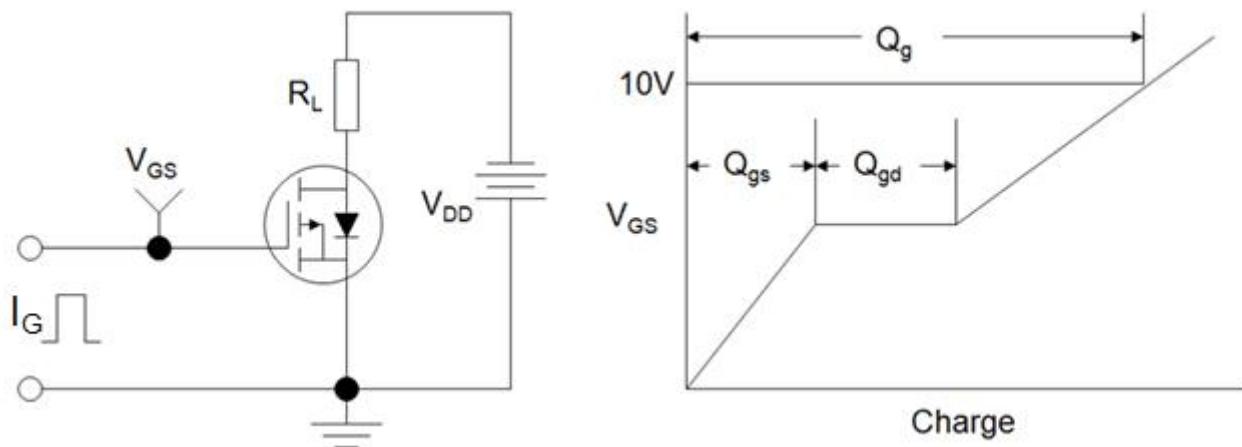
1. Repetitive Rating: Pulse width limited by maximum junction temperature

2. EAS condition : $T_J=25^\circ\text{C}$, $V_{\text{DD}}=-50\text{V}$, $V_{\text{GS}}=-10\text{V}$, $L=0.5\text{mH}$, $R_G=25\Omega$

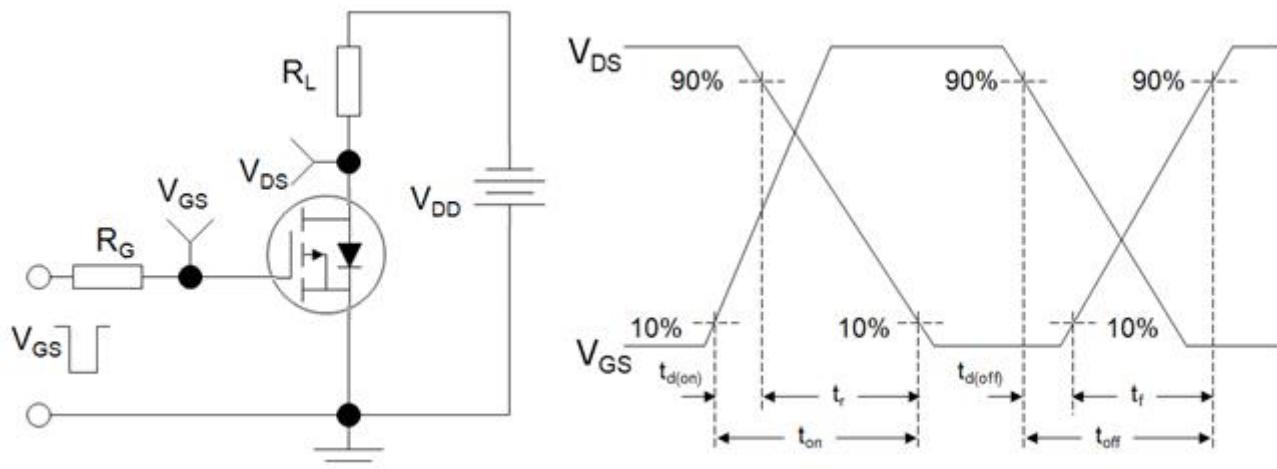
The table shows the minimum avalanche energy, which is 64mJ when the device is tested until failure

3. Identical low side and high side switch with identical R_G

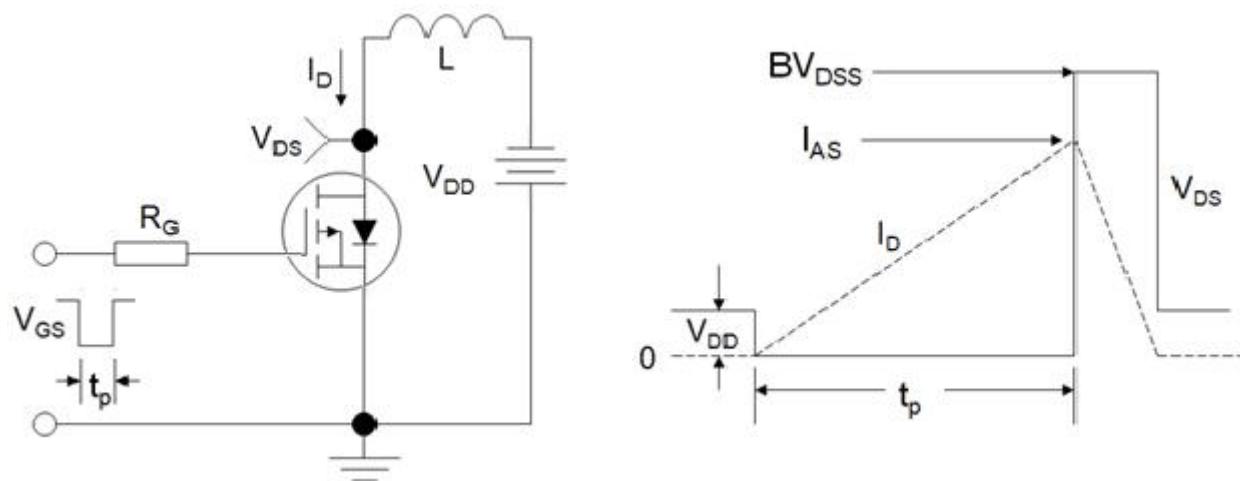
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 1. Output Characteristics

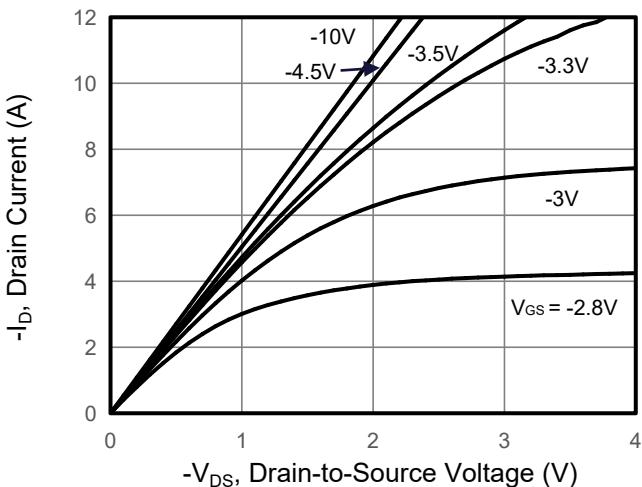


Figure 2. Transfer Characteristics

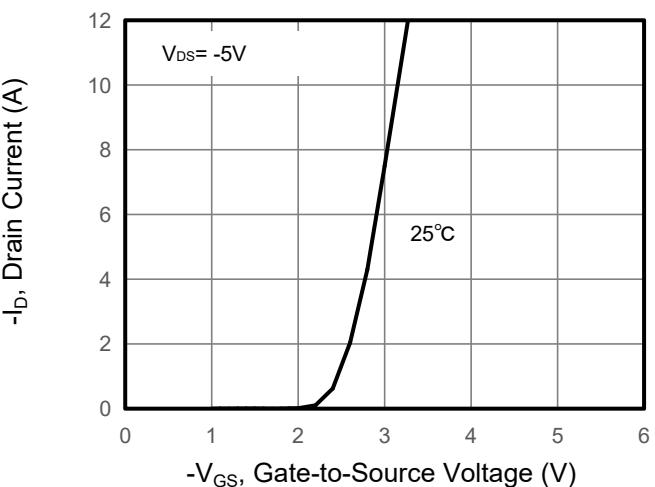


Figure 3. Drain Source On Resistance

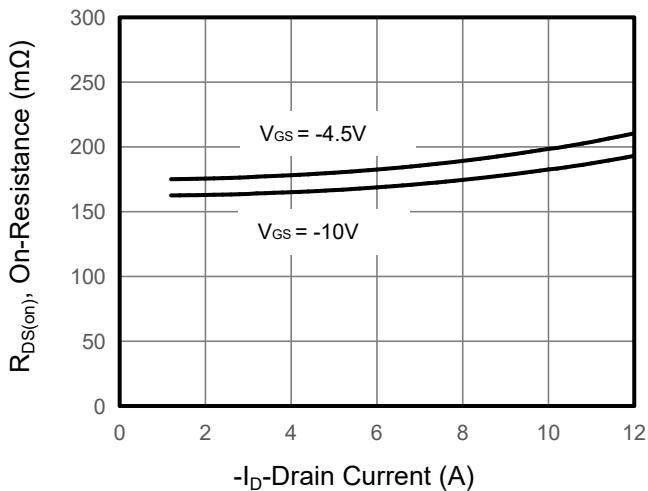


Figure 4. Gate Charge

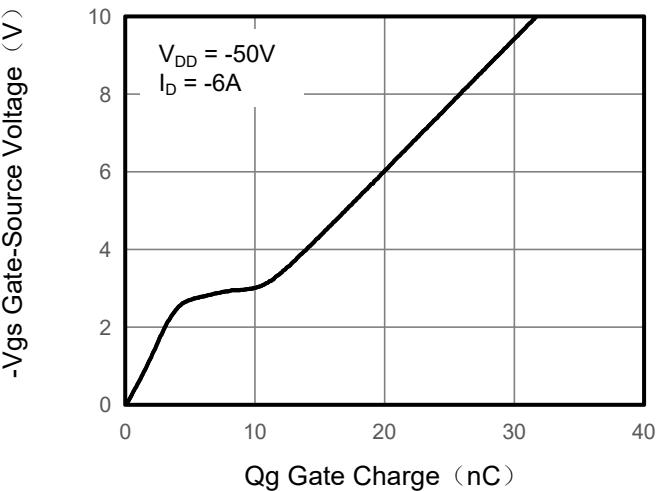


Figure 5. Capacitance

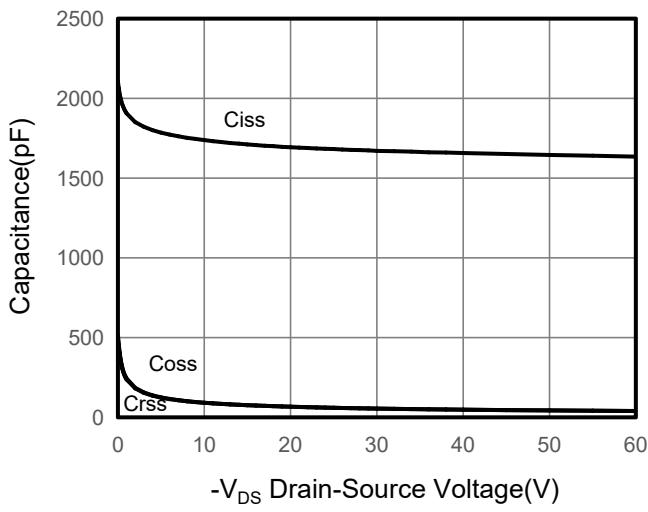
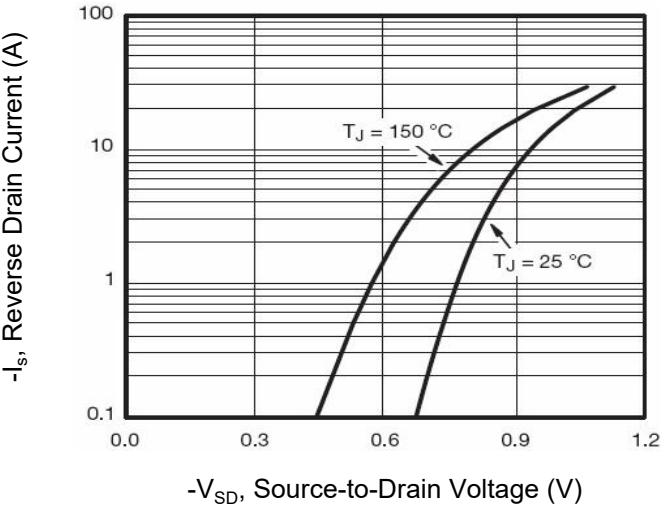


Figure 6. Source-Drain Diode Forward



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 7. Drain-Source On-Resistance

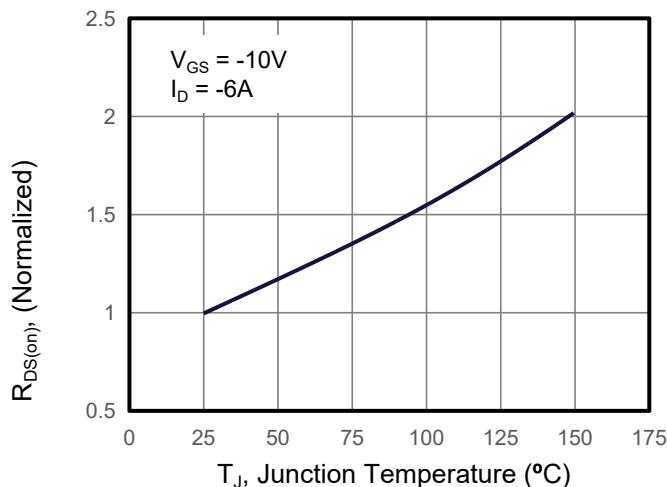


Figure 8. Safe Operation Area

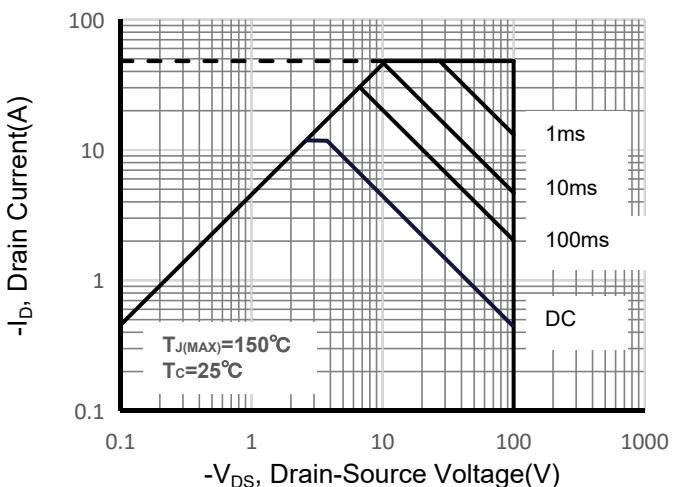


Figure 9. Maximum Continuous Drain Current vs Case Temperature

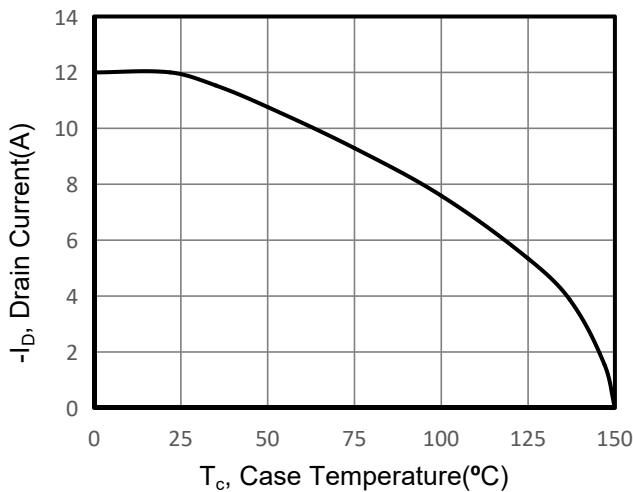
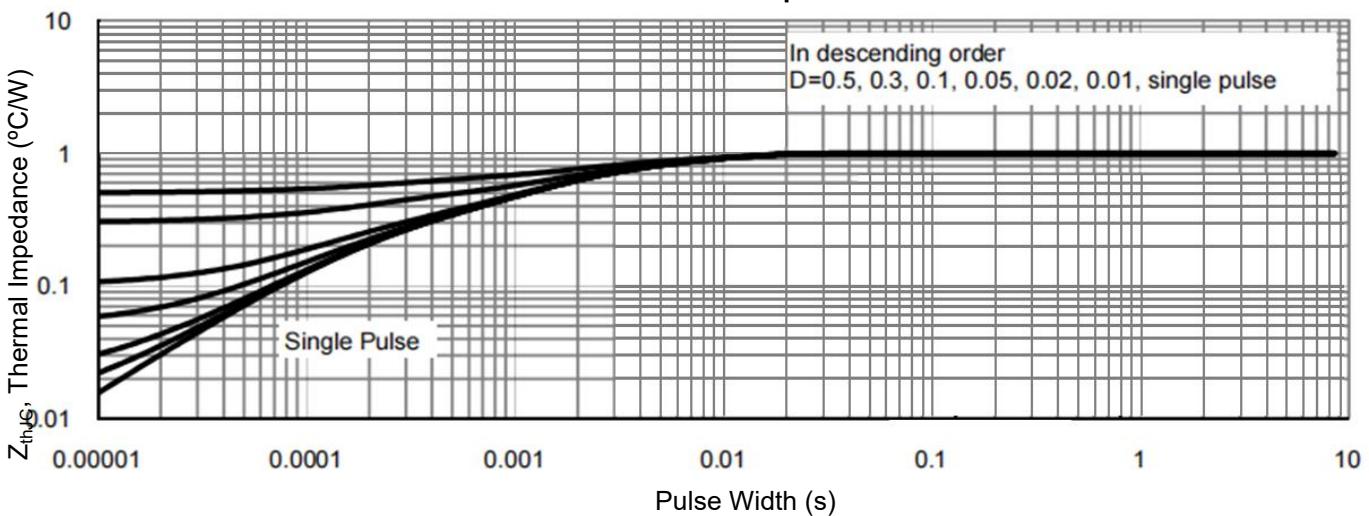
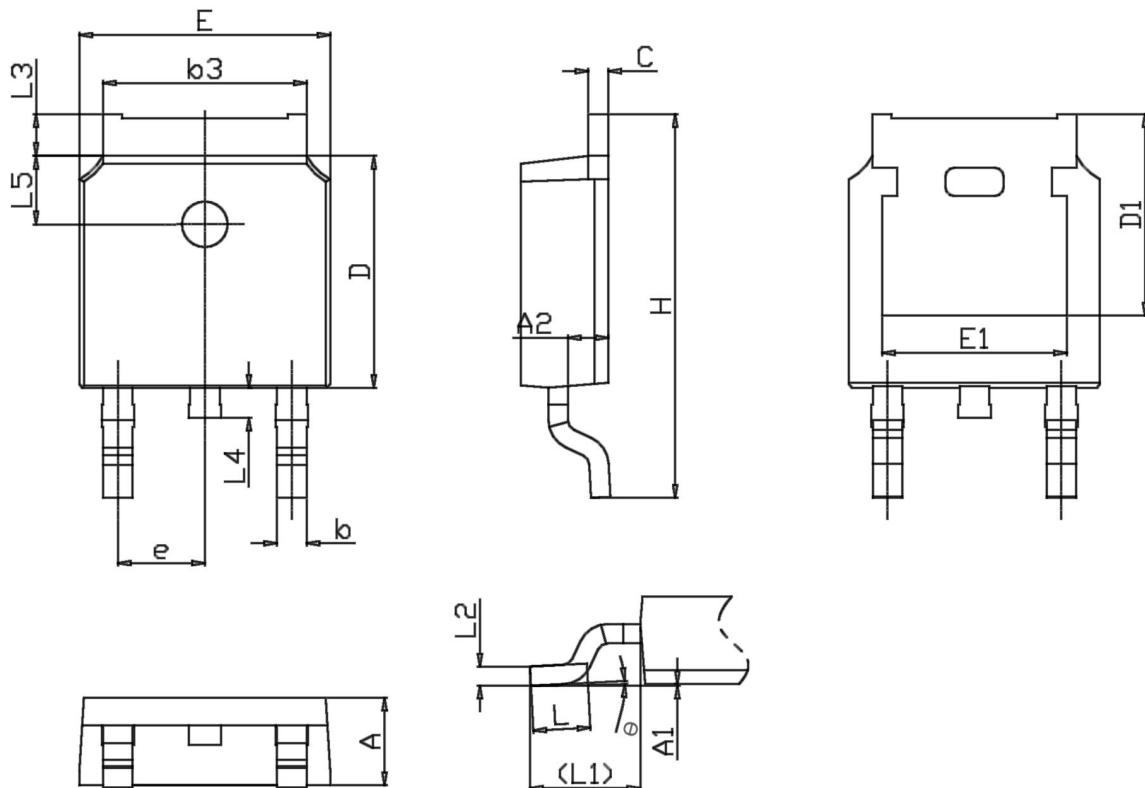


Figure 10. Normalized Maximum Transient Thermal Impedance



TO-252 Package Information



SYMBOL	mm		
	MIN	NOM	MAX
A	2.20	2.30	2.38
A1	0.00	-	0.12
A2	0.97	1.07	1.17
b	0.68	0.78	0.90
b3	5.20	5.33	5.46
c	0.43	0.53	0.61
D	5.98	6.10	6.22
D1	5.30REF		
E	6.40	6.60	6.73
E1	4.63	-	-
e	2.286BSC		
H	9.40	10.10	10.50
L	1.38	1.50	1.75
L1	2.90REF		
L2	0.51BSC		
L3	0.88	-	1.28
L4	0.50	-	1.00
L5	1.65	1.80	1.95
Θ	0°	-	8°